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GOVERNMENT OF INDIA
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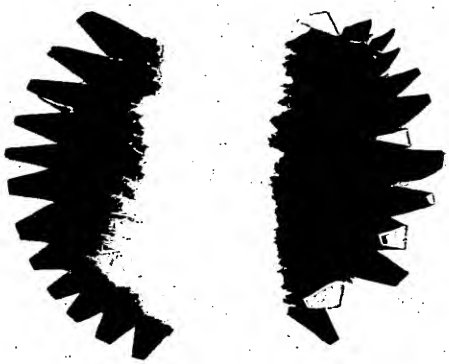
NEW DELHI - 110 008.

I, the undersigned, being an officer duly authorized in accordance with the provision of the Patent Act, 1970 hereby certify that annexed hereto is the true copy of the ***Application, Complete Specification*** *and* ***Drawing Sheets*** *filed in connection with Application for Patent No.* ***1021/Del/2002*** *dated* ***7th October 2002.***



Witness my hand this 30th Day of September 2003.

(S.K. PANGASA)
Assistant Controller of Patents & Designs

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1021-2

- 7 OCT 2002

FORM 1

THE PATENTS ACT, 1970
(39 of 1970)
APPLICATION FOR GRANT OF A PATENT
(See Sections 5(2), 7, 54 and 135)

1. I/we.

STMicroelectronics Pvt. Ltd., an Indian company, of Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 3001, Uttar Pradesh, India.

2. hereby declare –

(a) that I am/we are in possession of an invention titled *"An Improved Latch Type Sense Amplifier."*

(b) that the ~~provisional~~ / complete specification relating to this invention is filed with this application

(c) that there is no lawful ground of objection to the grant of a patent to me/us.

3. further declare that the inventor(s) for the said inventions is/are

(i) GUPTA Anuj, an Indian citizen, of 404 Mavilla, Mayur Vihar, Phase – I, Delhi – 110 091, India.

(ii) CHOPRA Sanjeev, an Indian citizen, of 91, Dilbagh Nagar, Basti Guzan, Jalandhar – 144 002, Punjab, India.

DUPLICATE

4. I/we claim the priority from the application(s) filed in convection countries, particulars of which are as follows: **NA**

5. I/we state that the said invention is an improvement in or modification of the invention the particulars of which are as follows and of which I/we are the applicant/patentee: **NIL**

6. I/we state that the application is divided out of my/our application, the particulars of which are given below and pray that this application be deemed to have been filed on under section 16 of the Act. **NIL**

7. That I am/we are the assignee or legal representative of the true and first inventors.

8. That my/our address for service in India is as follows:

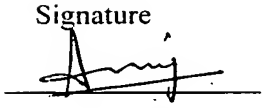
ANAND & ANAND, Advocates
B-41, Nizamuddin East
New Delhi – 110 013

Tel Nos.: (11) 4355078, 4355076, 4350360
Fax Nos.: (11) 4354243, 4352060

9- I/We the true and first inventors of this invention or the applicant(s) in the convention country declare that the applicant(s) herein is/are my/our assignee or legal representative.

a) *Anuj Gupta an Indian National of 404 Mavilla, Mayur Vihar, Phase-1, Delhi-110091*

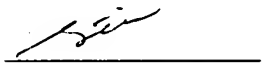
Signature



Dated this 7th day of October 2002

b) Sanjeev Chopra an Indian National of 91, Dilbagh nagar, Basti guzan, Jalandhar-144002, Punjab

Signature



Dated this 7th day of October 2002

10- that to the best of my/our knowledge, information and belief the fact and matters stated herein are correct and that there is no lawful ground of objection to grant of patent to me/us on this application.

11- Following are the attachment with the application

(a) Complete specification (3 copies)
(b) Abstract
(c) Formal drawings
(d) Power of Attorney
(e) Form 1 (in triplicate)
(f) Form 3 (in duplicate)
(g) Fee Rs. 5000/- In cash/cheque/bank draft bearing no. , date On Bank.

I/We request that a patent may be granted to me/us for the said invention.

Dated this 7th day of October 2002

Signature
STMicroelectronics Pvt. Limited

To

The Controller of Patents
The Patent Office, Delhi

02-IND-073

Form 2

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- 7 OCT 2002

THE PATENTS ACT, 1970

COMPLETE SPECIFICATION

SECTION 10

'AN IMPROVED LATCH TYPE SENSE AMPLIFIER'

ORIGINAL

***STMicroelectronics Pvt. Ltd.**, Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 3001, Uttar Pradesh, India, an Indian Company*

The following specification particularly describes and ascertains the nature of this invention and the manner in which it is to be performed:

AN IMPROVED LATCH TYPE SENSE AMPLIFIER

Field of the Invention

The present invention relates in general to latch type sense amplifiers and more particularly provides an improved apparatus for a latch type sense amplifier for sensing low voltage splits with very high reliability.

Background of the invention

Sense amplifiers are used in memory devices for sensing the output voltage of selected memory cells. With advancements in technology, memory cells are continually shrinking in size. The reduction in memory cell size is accompanied by reduction in the sensed voltage from the memory cell. Conventional sense amplifiers are unable to provide reliable operation under these conditions.

Consider the conventional latch type sense amplifier of **Figure 1**. PMOS transistor **10**, PMOS transistor **20**, NMOS transistor **30** and NMOS transistor **40**, together form the memory latch. Bit line BL is connected through PMOS transistor **50** to the latch while complementary bit line BLB is connected through PMOS transistor **60**. Latch enable transistor **70** is connected to the control signal SAEN. The PMOS pass transistors **50 and 60** are cut-off as soon as the latch enable transistor is turned on. The problem with this arrangement is that the split required for latching correct data with sufficiently high reliability is dependent on two important criteria ---- the threshold voltage mismatch between the NMOS sense transistors **30 and 40** in the latch, and the capacitance imbalance which may exist between the internal nodes (SN1 & SN2) of the sense amplifier. Since the sources of NMOS transistors **30 and 40** are connected together, the transistors go into saturation when an enable is provided. The current through them is therefore proportional to their respective V_{gs} - V_{th} values. Since the source of the two transistors is charged to the same potential therefore, the minimum bit line split required for latching correct data is required to be greater than the threshold voltage mismatch between them. In other words, the minimum voltage differential between the inputs necessary for the correct latching of data is largely determined by the threshold voltage mismatch present between the NMOS transistors 30 and 40 forming the latch. Triggering the sense amplifier at a voltage differential equal to the minimum required voltage results in large access times, which limits the speed of the device. High-speed memory designs are not feasible with such an arrangement. This implies that a greater voltage split on the bit lines is

required to offset such effects. As the discharge rate is slow in high-density memories, even a few extra milli volts of split result in an increase in the overall access time.

US patent 4910713 describes a general-purpose sense amplifier suited for memory and level shifting applications. In this conventional circuit arrangement, the amount of voltage split necessary for the correct data to be latched is largely governed by the threshold voltage mismatch present in the NMOS transistors forming the latch. Triggering the sense amplifier at such a voltage split results in larger access times, which ultimately proves to be a bottleneck in high speed memory designs. A further disadvantage is that this type of a sense amplifier is not very reliable when the voltage difference between the bitlines is small.

US patent 6181621 describes a threshold voltage mismatch compensated sense amplifier for SRAM arrays. The disadvantage of the circuit described by this invention is that it is complex involving more number of transistors, which require more signals to operate. Coordination of the many signals used in the invention is cumbersome.

Object and summary of the invention

The object of this invention is to overcome the drawbacks mentioned above and provide an improved Sense Amplifier that offers reliable sensing of low voltage differences thereby enabling high-speed memory cell operation.

Another object of the invention is to reduce the memory access times during a read operation.

Yet another object of the invention is to avoid glitches on the nodes of the sense amplifier.

To achieve the above objectives, this invention provides an improved latch type sense amplifier circuit. The modifications include delaying the disconnection of the pass transistors connecting the bit lines to the sense amplifier and providing additional transistors to reduce the effect of threshold mismatch between the NMOS transistors of two inverters forming the latch.

Brief description of accompanying drawings

The objects and advantages of the invention will become more apparent in reference to the following description and accompanying drawings, wherein:

Figure 1 illustrates the circuit diagram of a conventional latch type sense amplifier.

Figure 2 shows the circuit diagram of an improved latch type sense amplifier as provided by the present invention.

Figure 3 shows a timing diagram illustrating the operation of an improved latch type sense amplifier as provided by the present invention.

Figure 4 shows a graph illustrating the wave forms as produced during the operation of a conventional latch type sense amplifier.

Figure 5 shows a graph illustrating the wave forms as produced during the operation of an improved latch type sense amplifier as provided by the present invention.

Detailed Description

The present invention aims to overcome the above mentioned problem of larger access times in memories by triggering the sense amplifier at a voltage split less than what is required in the conventional scheme. The improved circuit is able to achieve a substantial improvement of around 15-20% in reliability for sensing low voltages as compared to the conventional circuits. This improved reliability further results in achieving a significant access time improvement.

Figure 1 shows the circuit diagram of a conventional latch type sense amplifier as used in the prior art and has already been described in the "Background of the invention" section.

The circuit in **Figure 2** illustrates an improved latch type sense amplifier as provided by the present invention. The circuit comprises a modified latch consisting of PMOS transistors **110**, **120**, NMOS transistor **130,140**, and an additional set of NMOS transistors **170,180**. The bit line BL is connected through a PMOS transistor **150** and the bit line BLB is connected through a PMOS transistor **160**. The NMOS transistor **200,** controlled by the SAEN signal, is used for enabling the latch. Delayed version of the SAEN signal, i.e. SAEND, is used to control the switching off of the PMOS pass transistors **150,160**. The signal SAEND is

generated in the present implementation from a pair of inverters **180,190**, though it may also be generated by various other means that can delay the signal.

The present invention modifies the basic latch of the sense amplifier to provide a mechanism that reduces the effect of threshold mismatch of the NMOS transistors 130 and 140 of inverters forming latch. This mechanism comprises two additional NMOS transistors **170** and **180** that are added in series with NMOS transistors **130 and 140** present in the latch portion of a conventional sense amplifier. Considering the situation prior to coming of SAEN signal, the sources of NMOS transistors **130,140** are charged to different potentials depending upon their respective threshold voltages. For the worst case mismatch, when SN2 discharges, the threshold voltage of transistor **130** may be more than the threshold voltage of transistor **140**. After SAEN goes high the transistors **130 and 140** operate in their saturation region while transistors **170 and 180** operate in their linear region. The drain-to-source resistance of transistor **180** is a function of the node voltage **SN2** while the drain-to-source resistance of transistor **170** is a function of the node voltage **SN1**. The situation is such that the drain-to-source resistance of transistor **180** increases with respect to drain-to-source resistance of transistor **170**, when **SN2** discharges, thus effectively reducing the current through non-discharging node in comparison to the current through discharging node even in the presence of mismatch in the NMOS transistors 130 and 140. This degenerative feedback of the additional NMOS transistors **170** and **180** operating in their linear region operating as ~~linear~~ voltage controlled resistors reduces the effect of threshold mismatch of transistors **130** and **140** of the latch.

The second modification uses a delayed version of the Sense Amplifier Enable (SAEN) signal to keep the bit lines connected to the sense amplifier for a small duration after it has been enabled. This delay enables the regenerative feedback of the cross-coupled inverters to amplify the signal from the bit lines and aid the latch operation. The effective bit line split is reinforced by the latching action. By the time PMOS pass transistors **150 and 160** are shut off, the voltage split is sufficient for correct data to be latched.

As shown in **Figure 3**, this modification also overcomes the effects of capacitive mismatch between the SN1 and SN2 nodes of two inverters as the much larger bit line capacitance swamps out the small capacitive difference as the internal nodes of the sense amplifier are effectively joined to the bit lines during the delay duration "D".

The delay also solves the problem of a glitch occurring on the sense amplifier internal nodes in the conventional circuit due to clock-feed through as shown in **Figure 4**. The glitch occurs on both the internal nodes and in the same direction but it may pose problem by reducing the effective split if the glitch on the discharging node is greater than the one on the non-discharging node.

As shown in **Figure 5**, the present invention avoids any glitch since the delay causes the latch to be enabled first and the PMOS pass transistors to be shut-off after some time.

The two improvements described above: a) providing a mechanism for compensating the threshold voltage of the inverters and b) providing a delayed version of the SAEN signal – can be applied independently or collectively to the design of the improved sense amplifier. The combination of both the improvements provides the best results.

The description of the present invention has been presented for purposes of illustration and is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art.

We claim:

1. An improved latch type sense amplifier for a memory array providing increased reliability in sensing small voltage differences comprising:
   - two cross coupled inverters forming a latch,
   - supply coupling means for selectively connecting the latch to a supply source, and
   - bit line coupling means for selectively connecting inputs of each inverter to the complimentary bit lines from the memory array

   characterized in that it includes:
   - delaying means for delaying the disconnection of the bit lines from the sense amplifier.

2. An improved latch type sense amplifier as claimed in claim 1, further including compensating means for correcting the offset between the inverters of the latch and the supply coupling means.

3. An improved latch type sense amplifier as claimed in claim 1, wherein supply coupling means is an NMOS transistor.

4. An improved latch type sense amplifier as claimed in claim 1, wherein the bit line coupling means a PMOS transistor connecting in series between each bit line and the latch.

5. An improved latch type sense amplifier as claimed in claim 2, wherein the compensating means is a pair of NMOS transistors connected between the NMOS transistors of the latch and the common supply terminal

6. An improved latch type sense amplifier as claimed in claim 2, wherein the supply coupling means is controlled by a strobe signal.

7. An improved latch type sense amplifier as claimed in claim 6, wherein the strobe signal to disable the supply coupling means is delayed by the delaying means.

8. An improved latch type sense amplifier as claimed in claim 1, wherein the delaying means includes a plurality inverters connected in series.

9. A method for improving a latch type sense amplifier for a memory array in order to increase reliability in sensing small voltage differences, comprising the steps of:

- cross coupling two inverters to form a latch,
- selectively coupling the latch to a supply source, and
- selectively coupling the inputs of each inverter to the complimentary bit lines from the memory array

characterized in that it includes the step of:

- delaying the disconnection of the bit lines from the sense amplifier until a short duration after the enabling of the sense amplifier latch.

10. A method for improving a latch type sense amplifier as claimed in claim 9, further including the step of correcting the offset mismatch between the inverters of the latch and the supply coupling means.

11. A method for improving a latch type sense amplifier as claimed in claim 10, wherein the offset correction is performed by providing degenerative feedback in the supply terminal path of the latch transistors that operate in the saturation mode.

12. A method for improving a latch type sense amplifier as claimed in claim 9, wherein the disconnection of the bit lines is delayed by utilizing a delayed version of the Sense Amplifier Enable signal to disconnect the bit lines.

13. An improved latch type sense amplifier for a memory array providing increased reliability in sensing small voltage differences substantially as herein described with reference to and as illustrated in figures 2, 3 & 5 of the accompanying drawings.

14. A method for improving a latch type sense amplifier for a memory array in order to increase reliability in sensing small voltage differences substantially as herein

described with reference to and as illustrated in figures 2, 3 & 5 of the accompanying drawings.

Dated this 7th day of October 2002

of **ANAND & ANAND, Advocates**
Agents for the Applicants

AN IMPROVED LATCH TYPE SENSE AMPLIFIER

Abstract of the Invention

The invention provides an improved latch type sense amplifier circuit comprising two cross coupled inverters forming a latch, supply coupling means for selectively connecting the latch to a supply source, and bitline coupling means for selectively connecting the inputs of each inverter to the complimentary bitlines from the memory array. The invention senses small voltage difference between the bitlines with improved reliability by providing a delayed sense amplifier enable signal to the PMOS pass transistors for delaying the disconnection of the bitlines from the sense amplifier until the latching action is completed, and adding two extra NMOS in series with the existing NMOS transistors of the conventional latch for correcting the offset between the thresholds of the inverters of the latch.

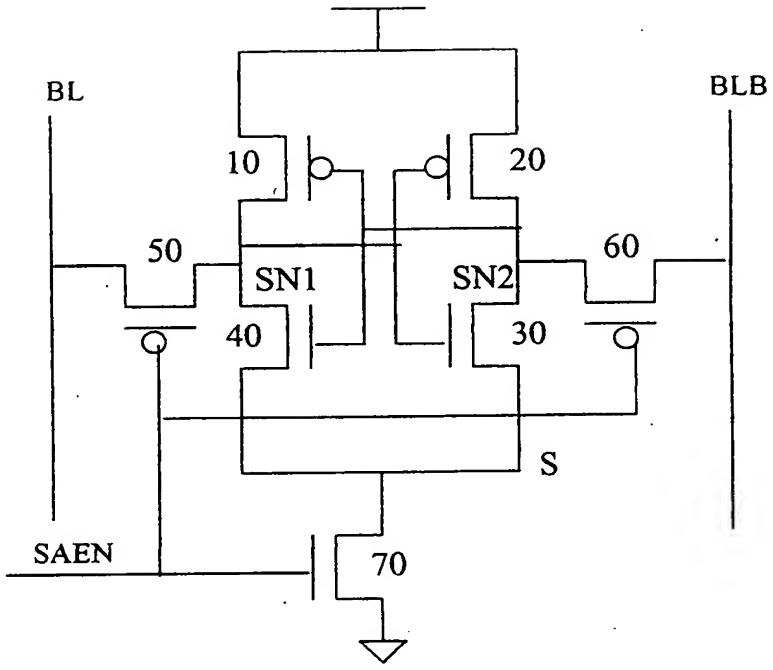

FIGURE 1

ORIGINAL

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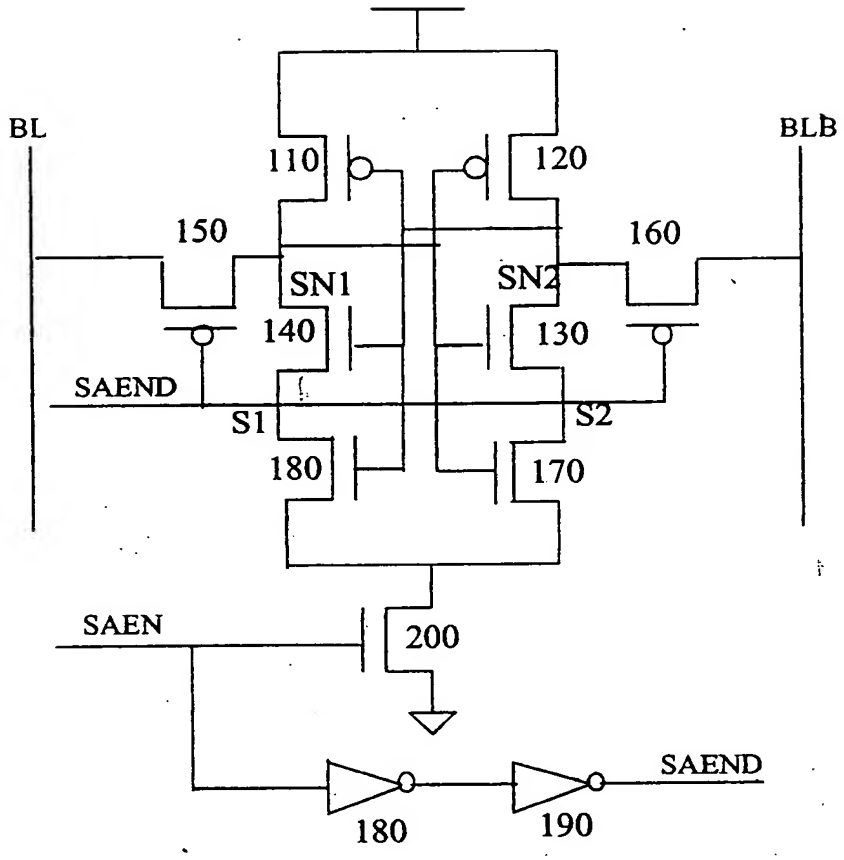

FIGURE 2

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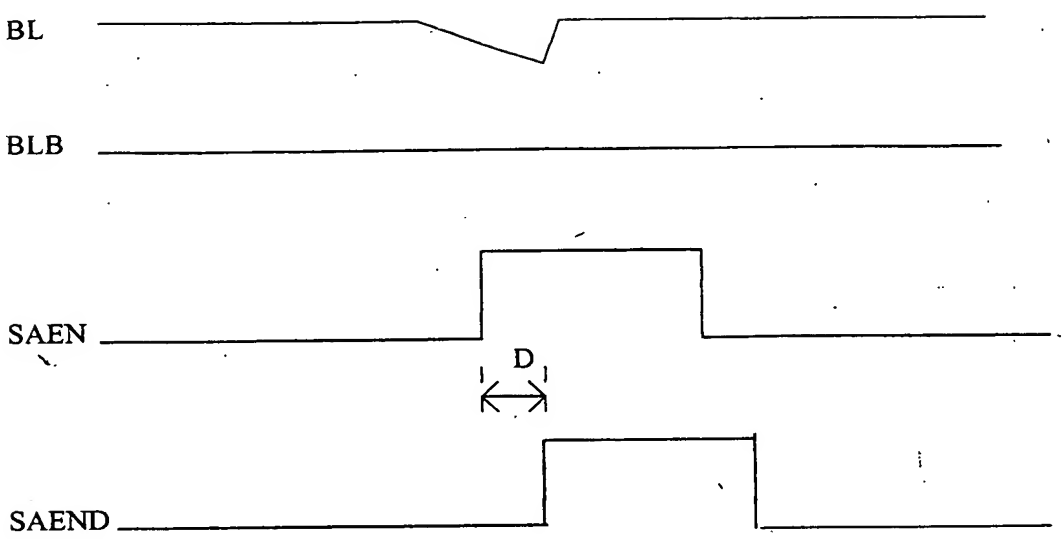

FIGURE 3

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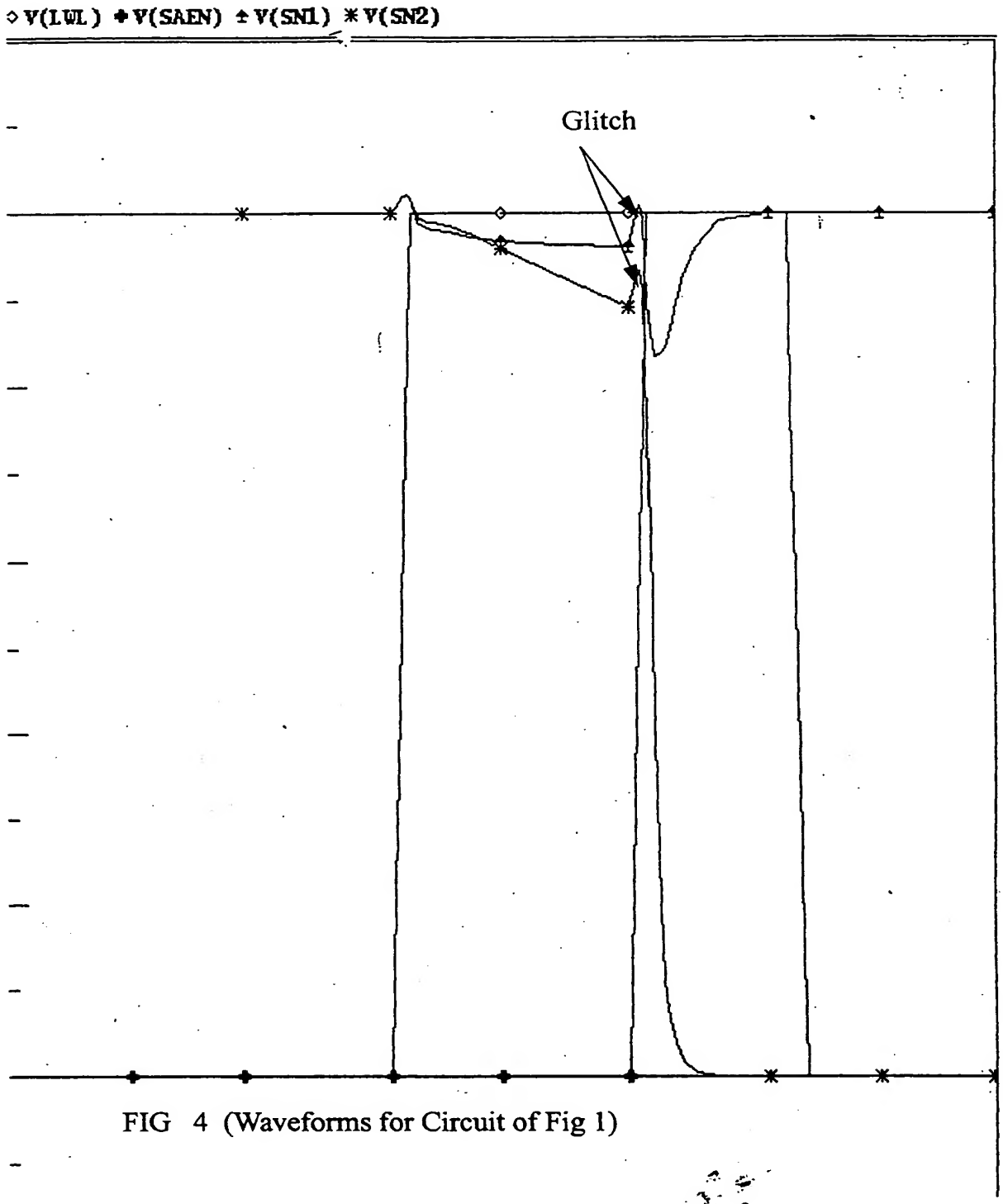

FIG 4 (Waveforms for Circuit of Fig 1)

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Attorney for the Applicant

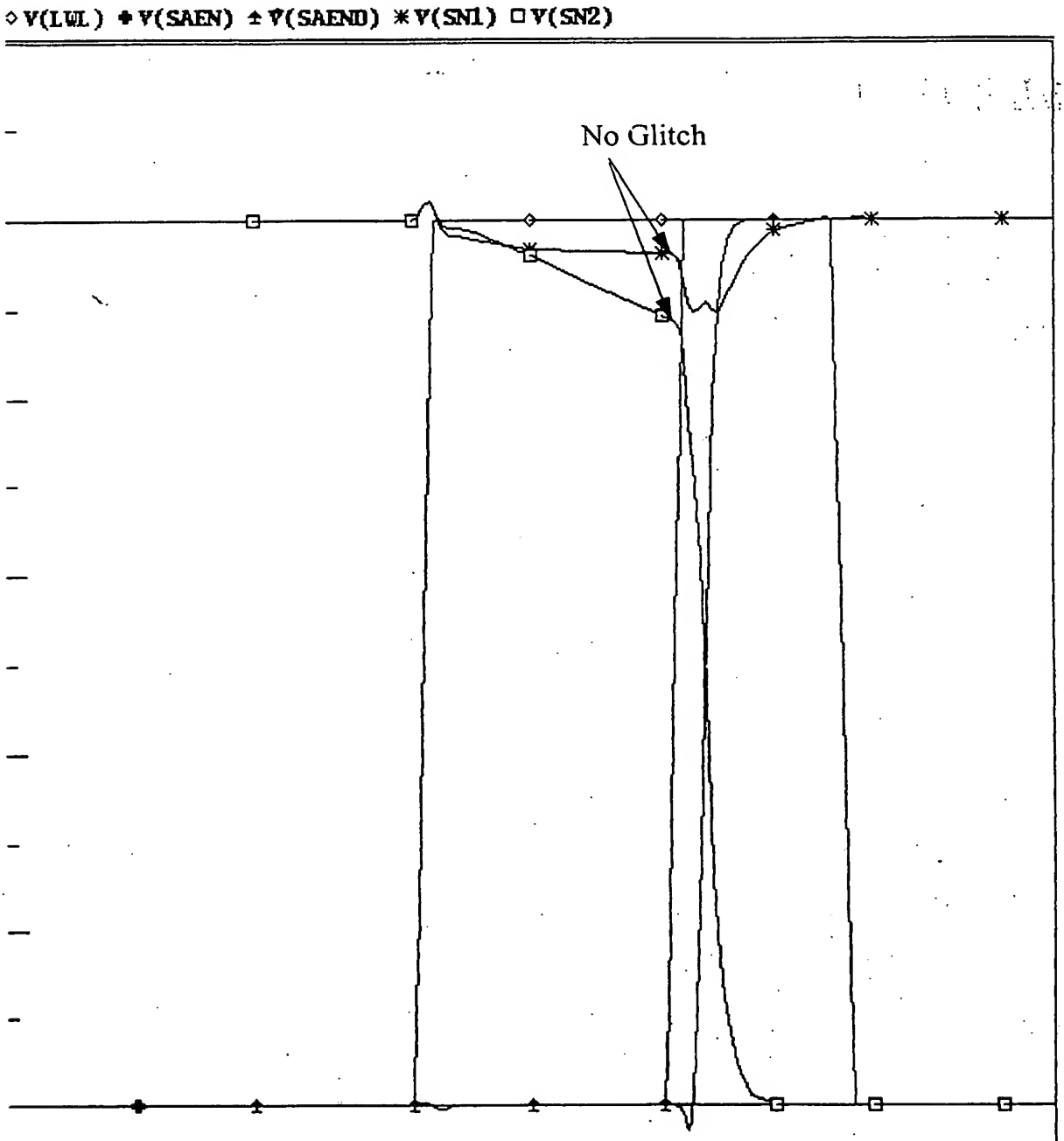

FIG 5 (Waveforms for Circuit of Fig 2)

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